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Fig. 1 is a plan view of a semiconductor device. The device is rectangular with a central square region 19. It features four rows of circular elements (12) connected by lines (13). The top and bottom rows are labeled 11 and 16, respectively. The left and right rows are labeled 14a and 14, respectively. A dashed line II-II passes through the center. Other labels include 17, 15, and 15a.

[illegible]



FIG. 3A

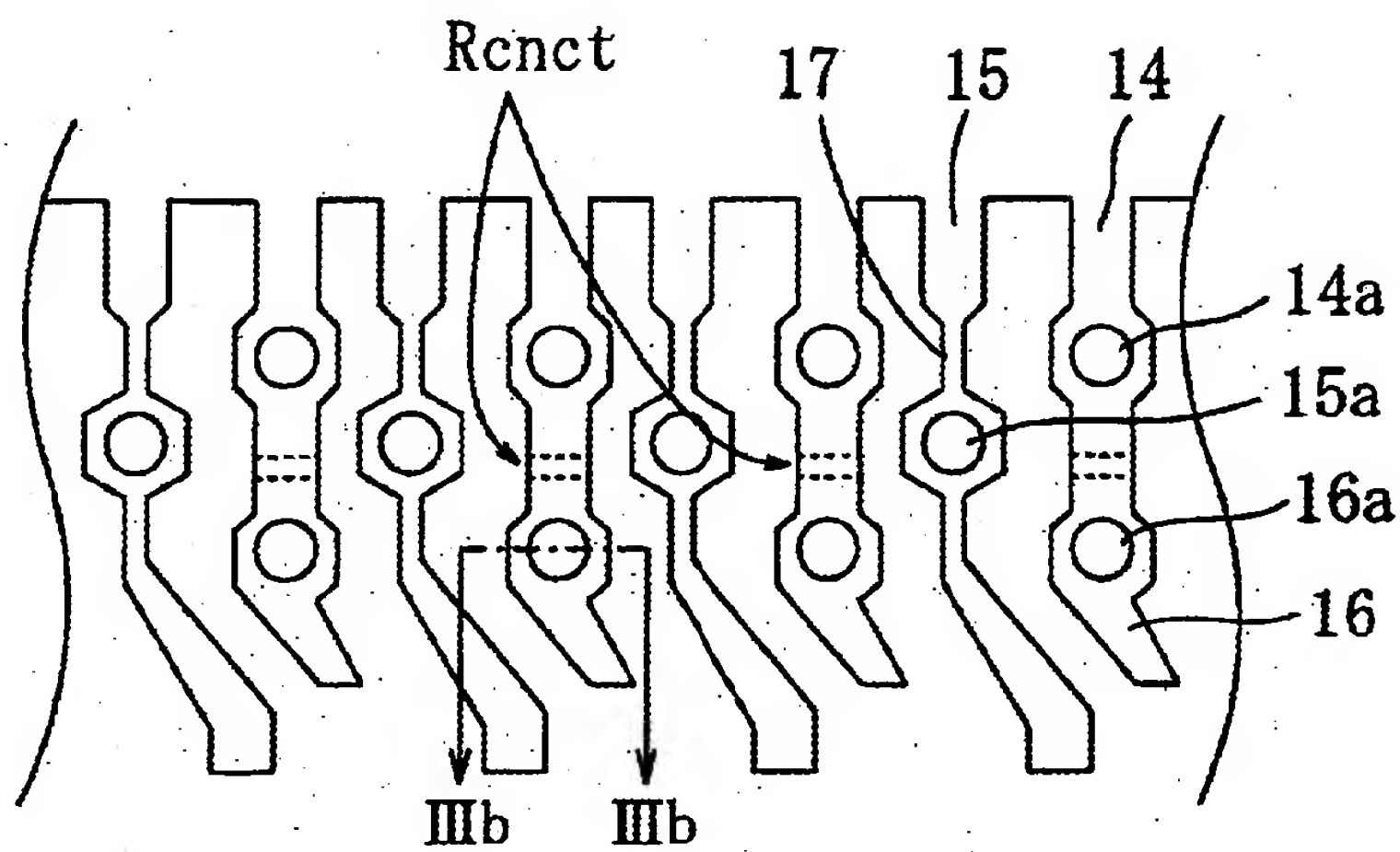


FIG. 3B

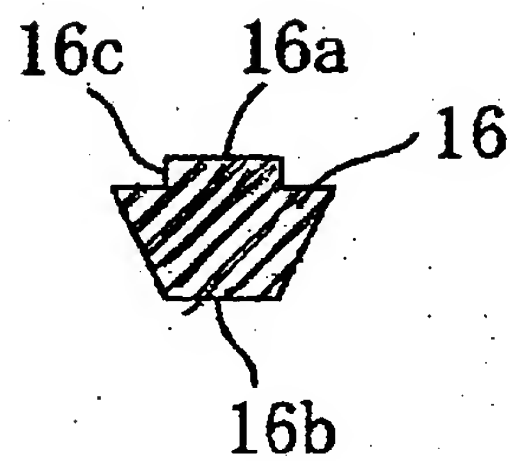




FIG. 4A

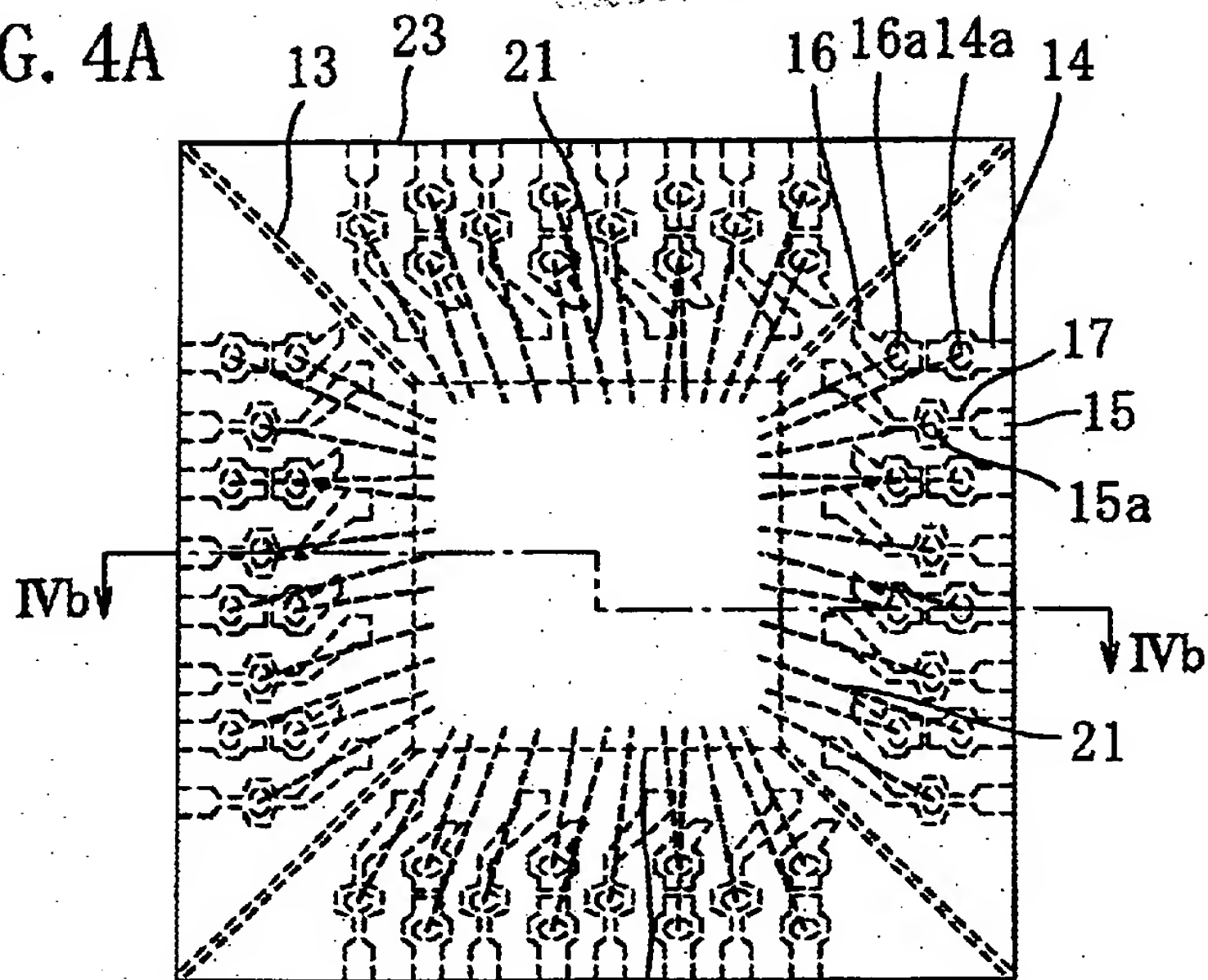


FIG. 4B

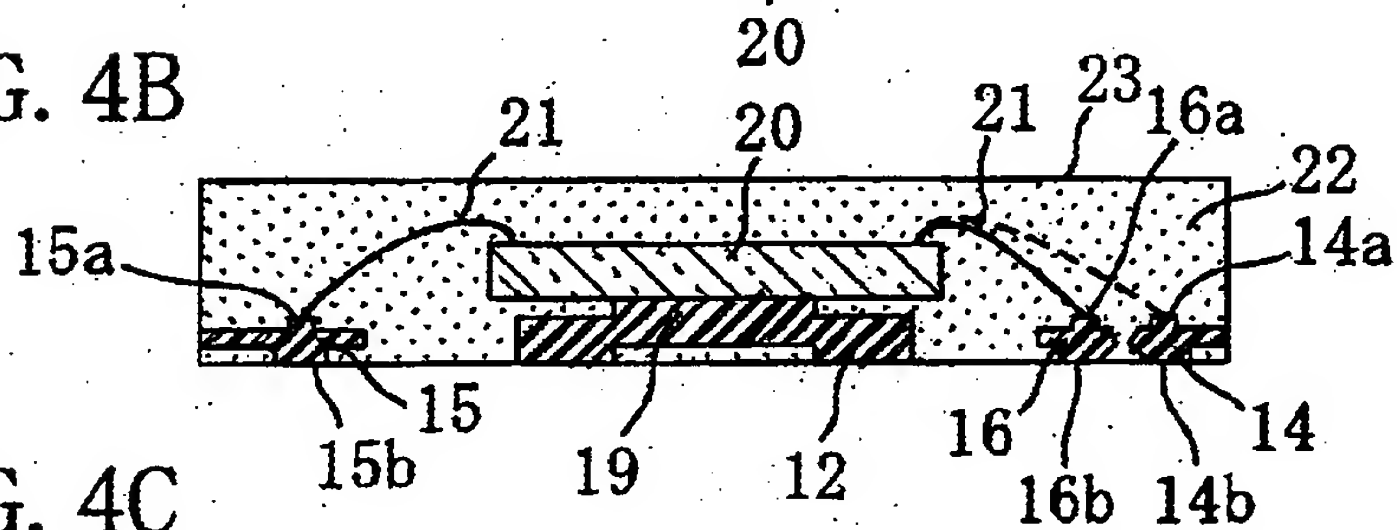


FIG. 4C

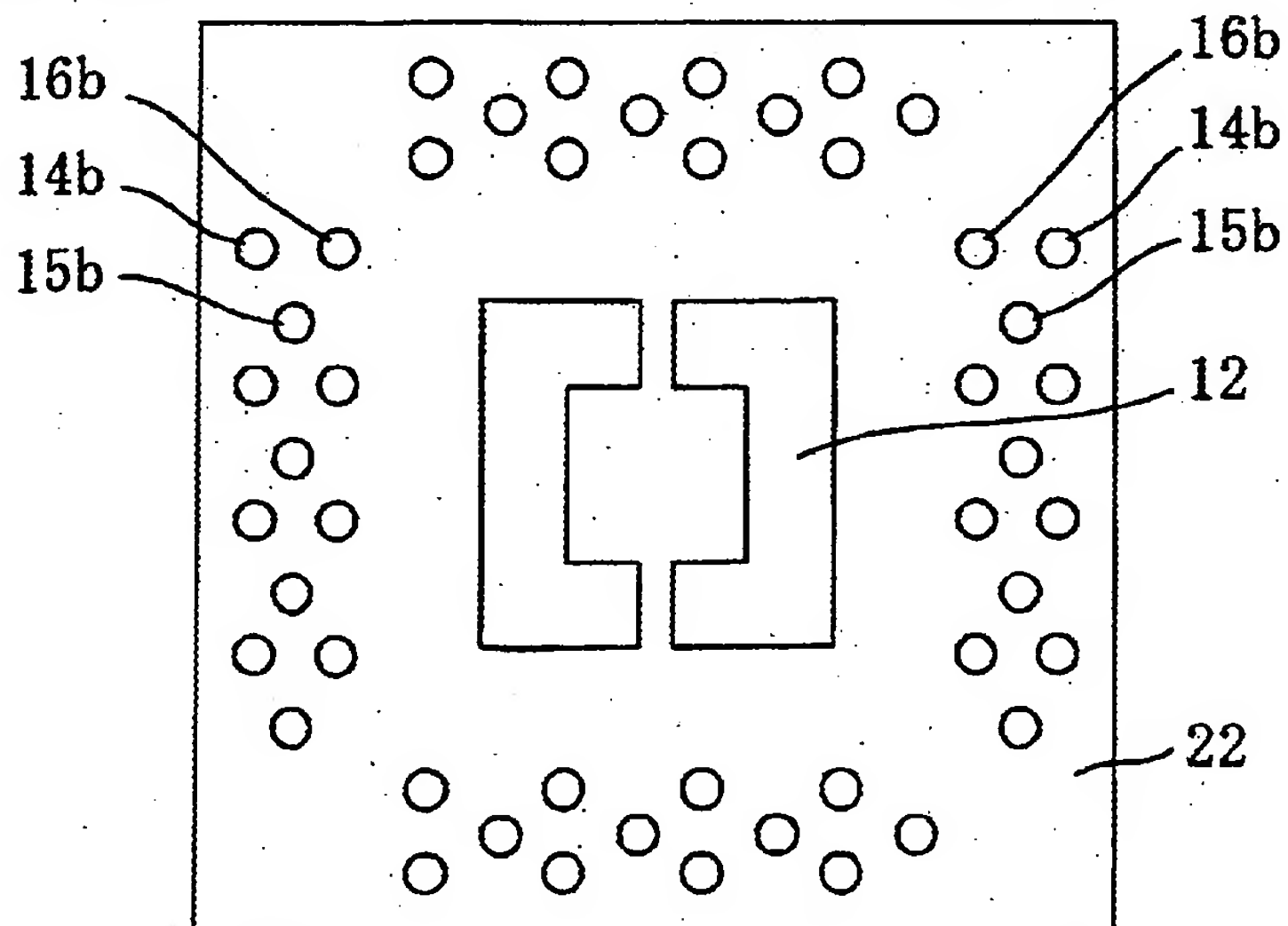




FIG. 5A

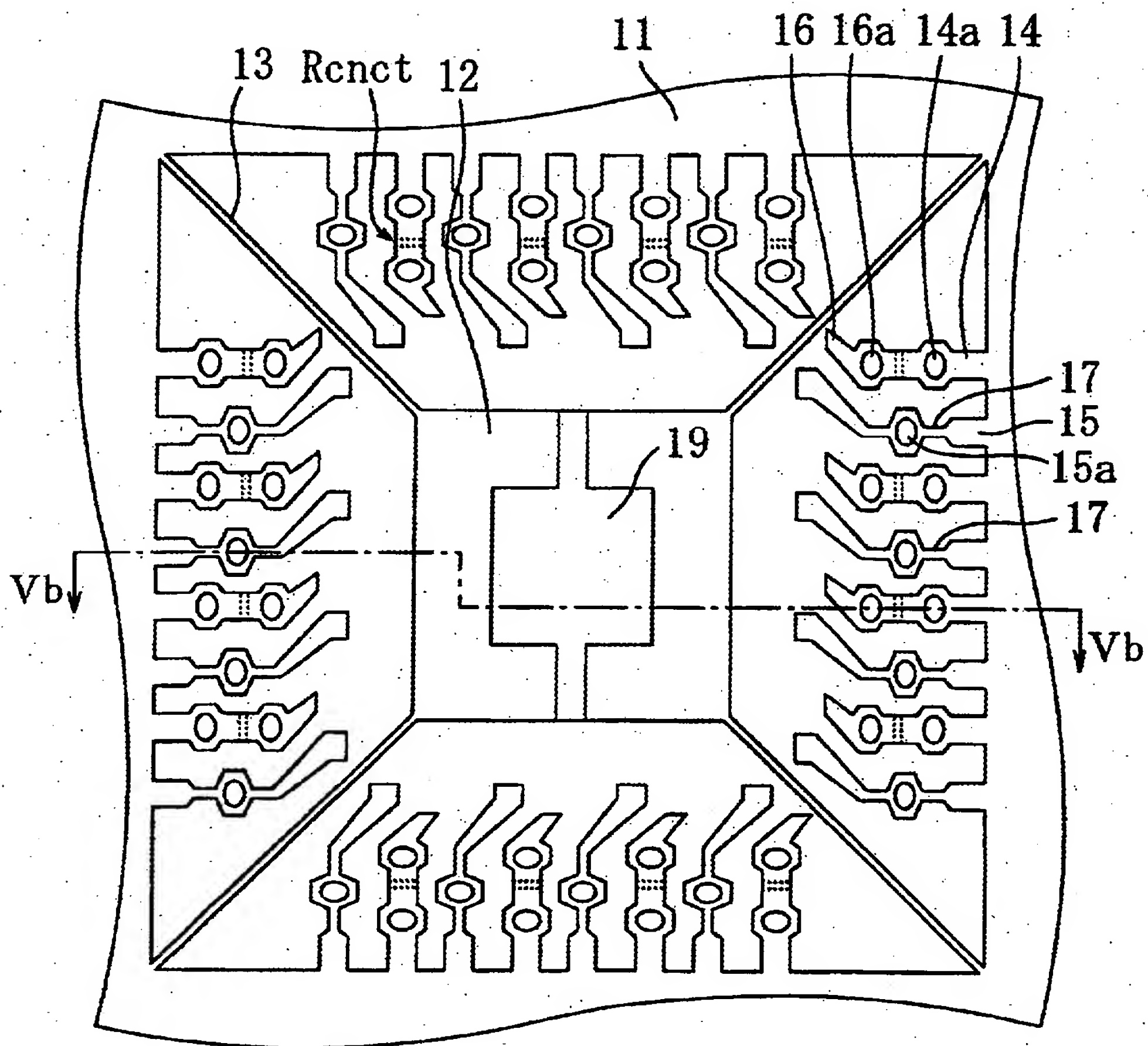


FIG. 5B

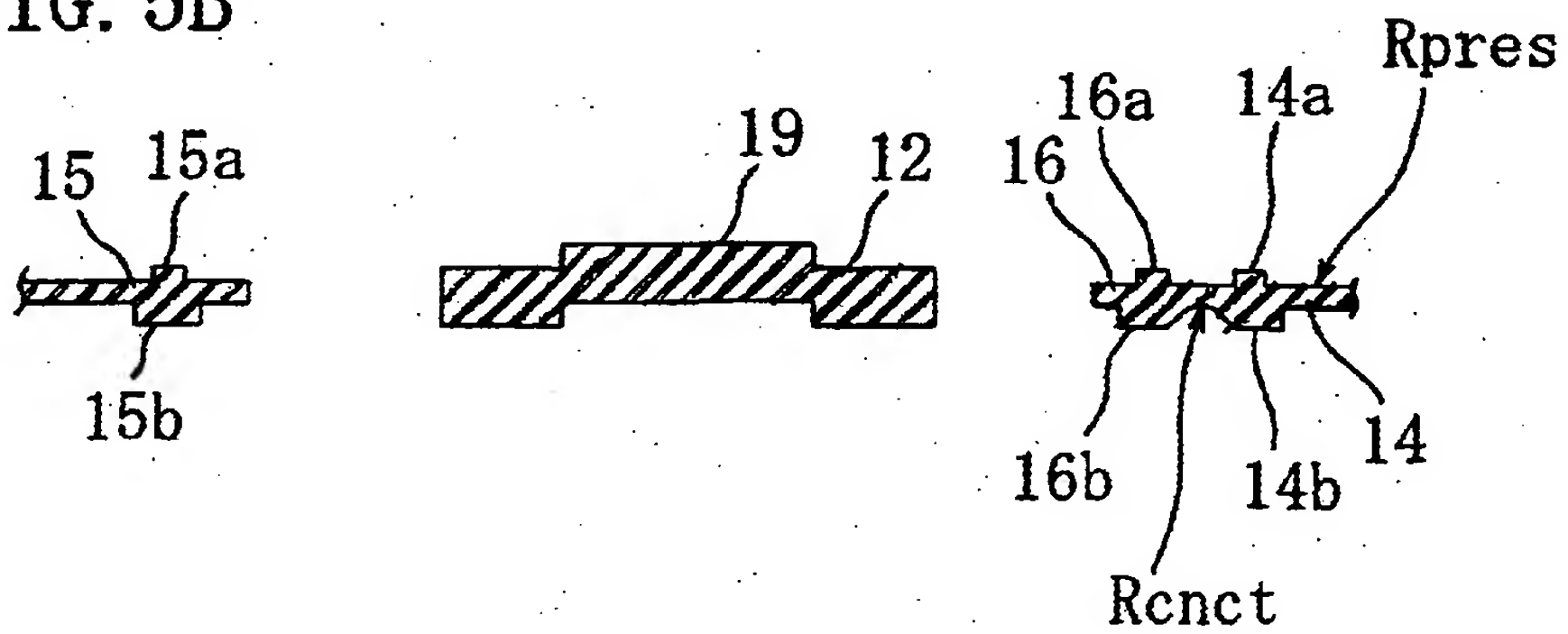




FIG. 6A

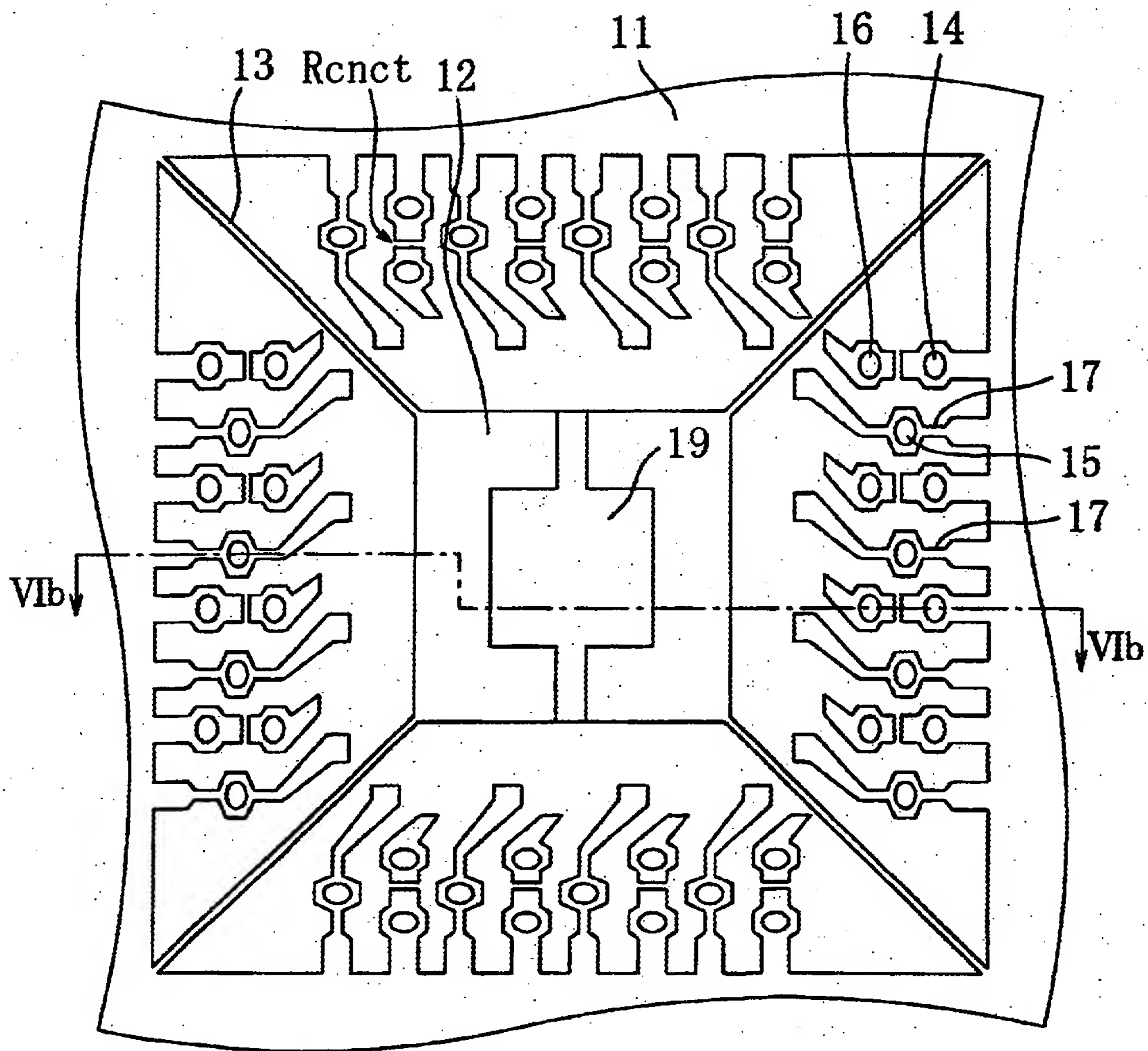


FIG. 6B

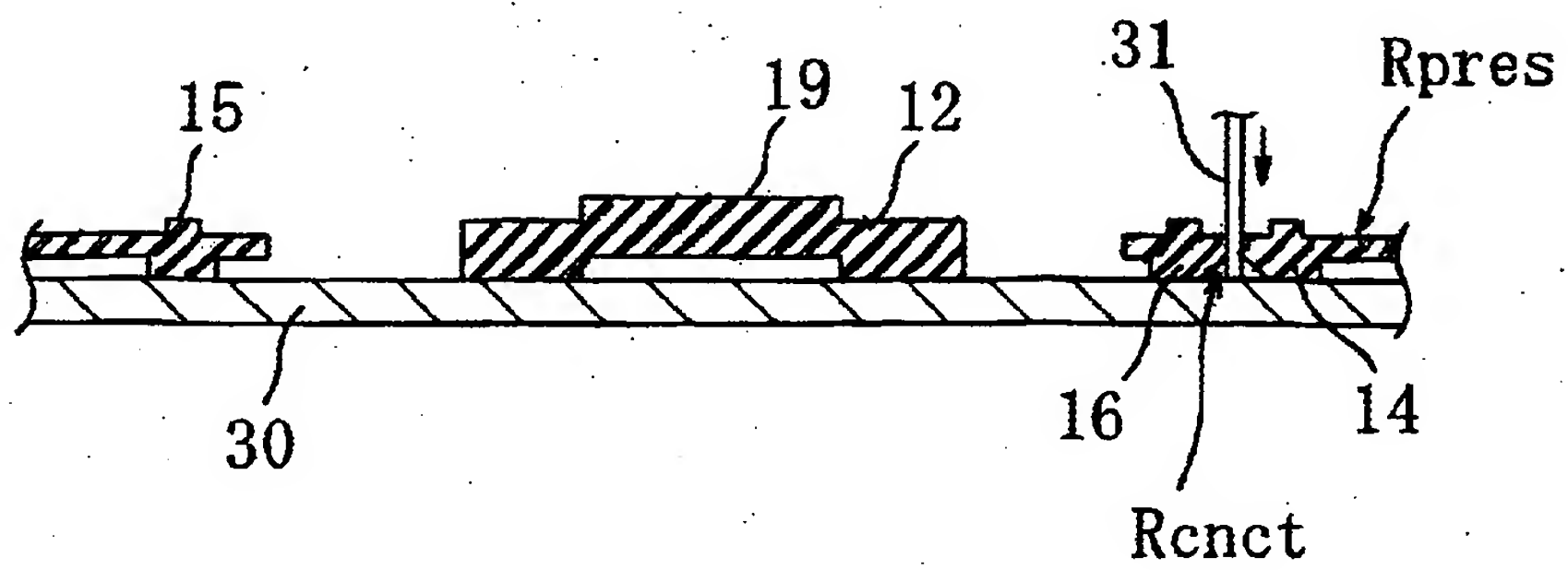




FIG. 7A

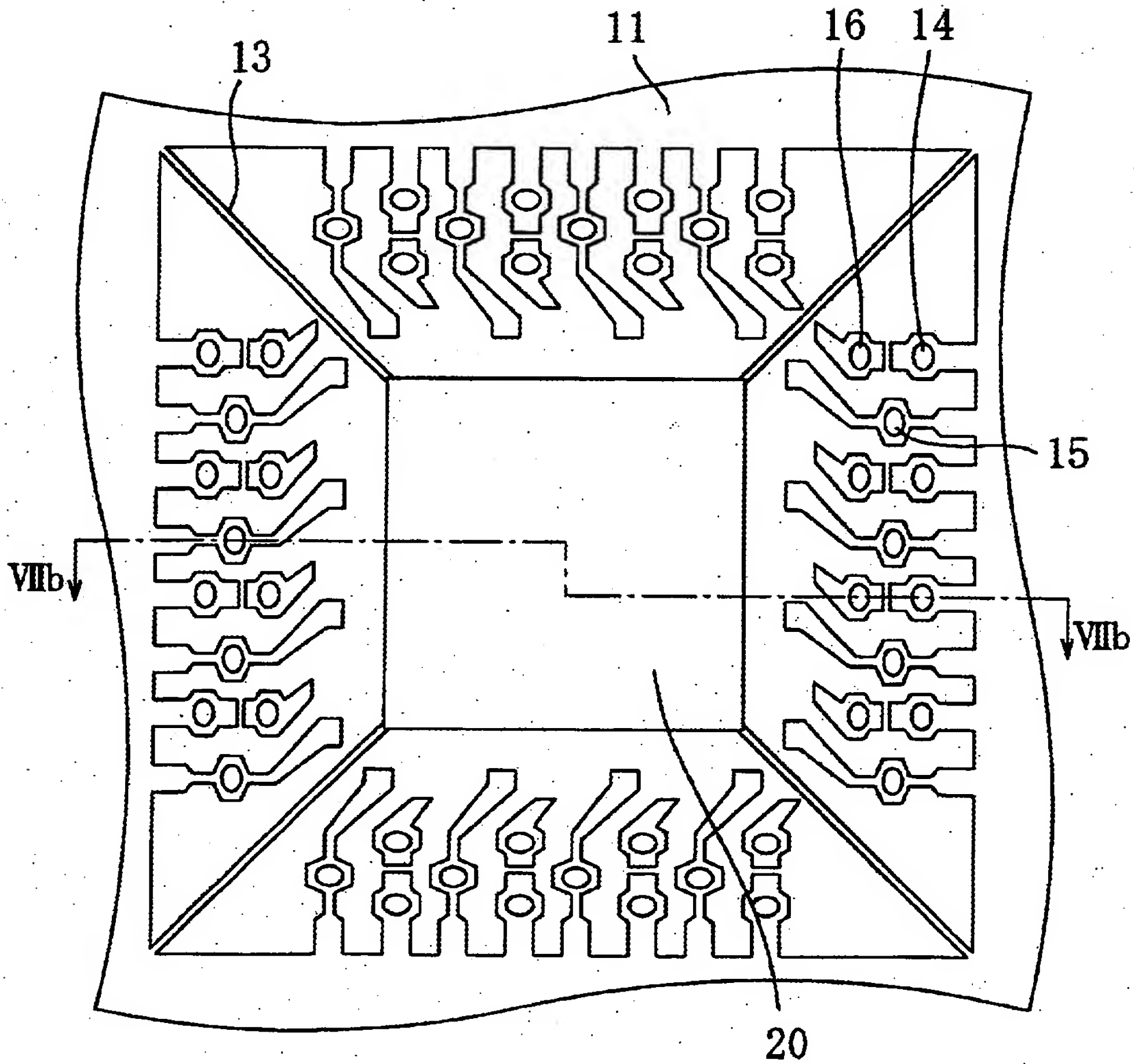


FIG. 7B

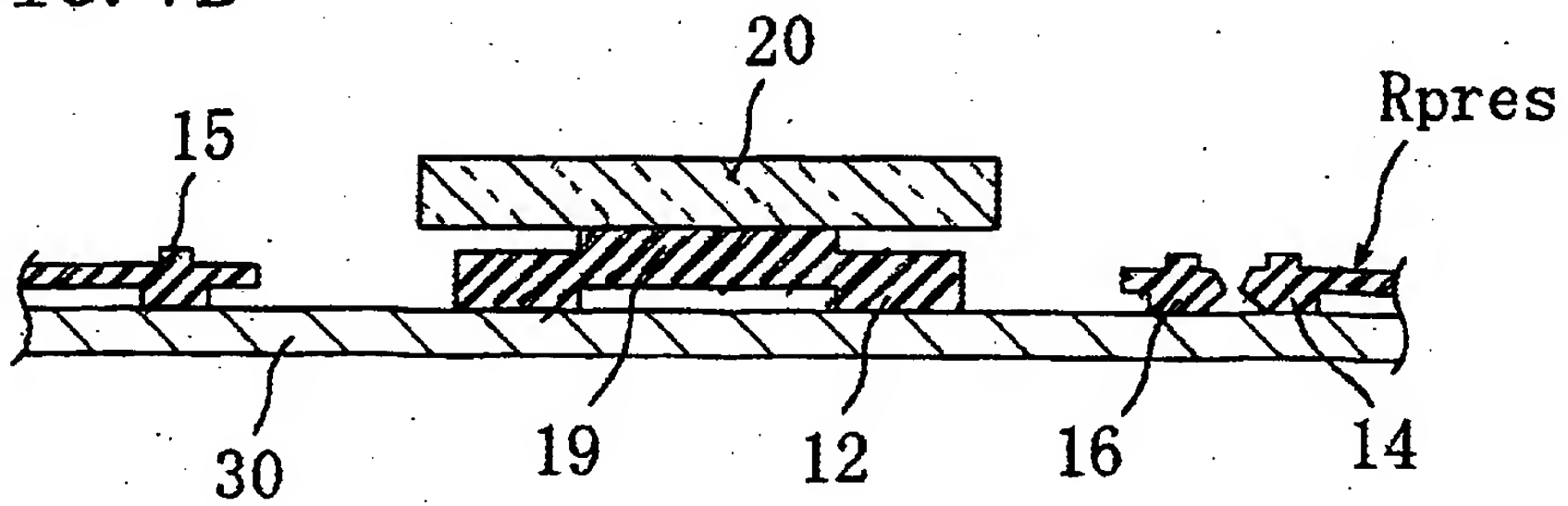




FIG. 8A

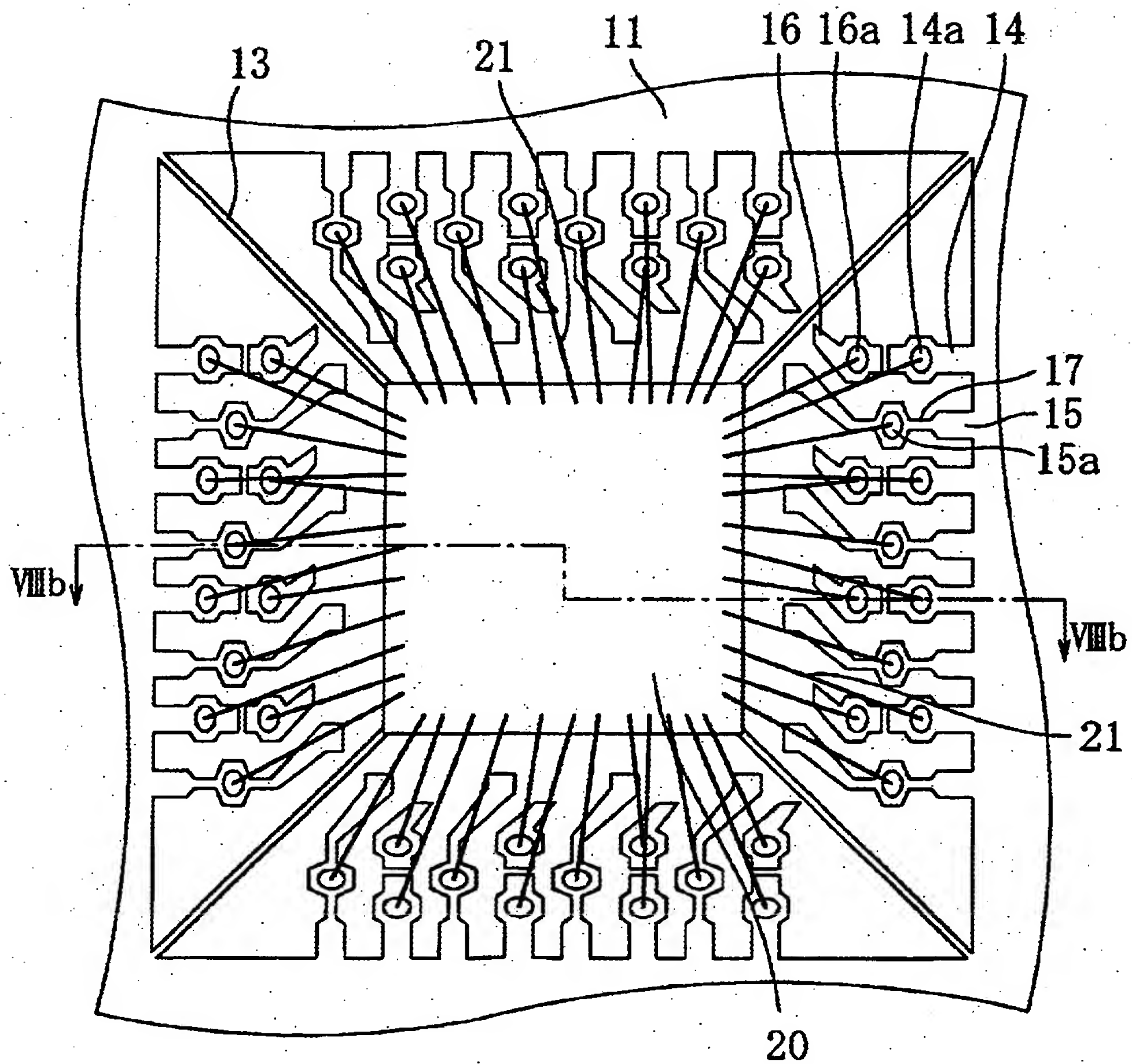


FIG. 8B

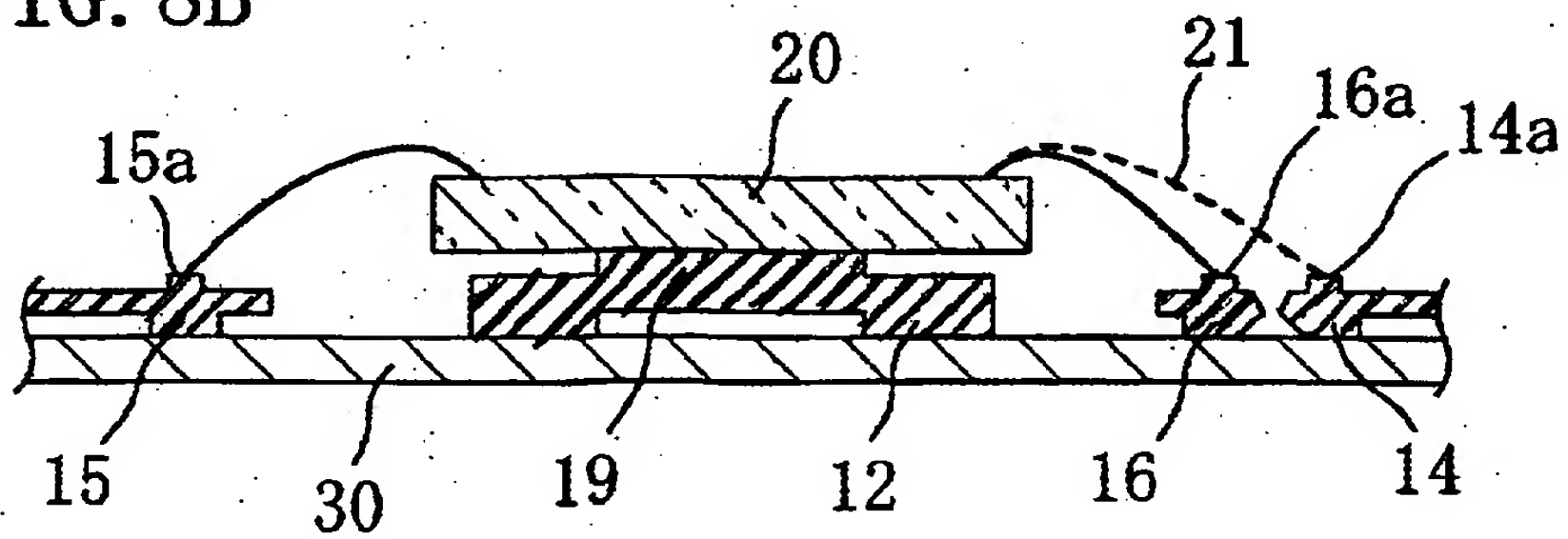




FIG. 9A

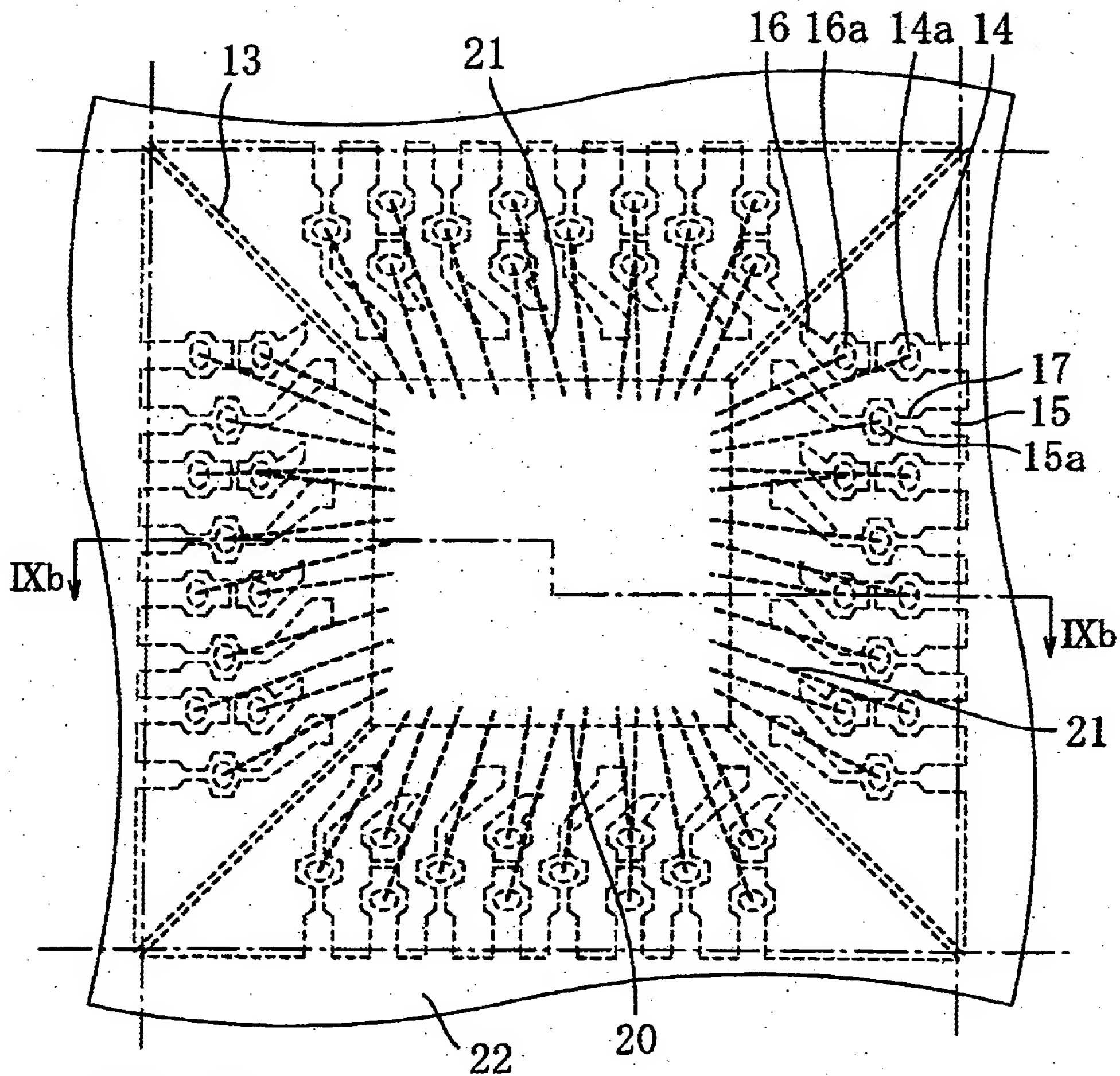


FIG. 9B

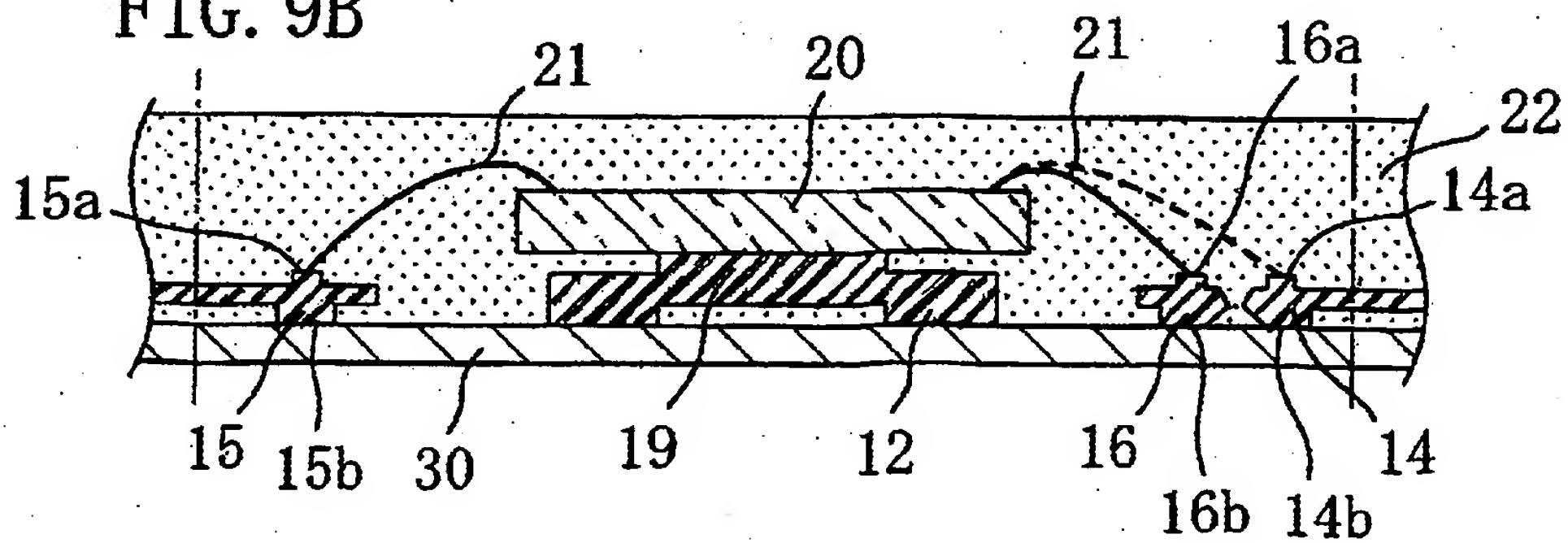




FIG. 10A

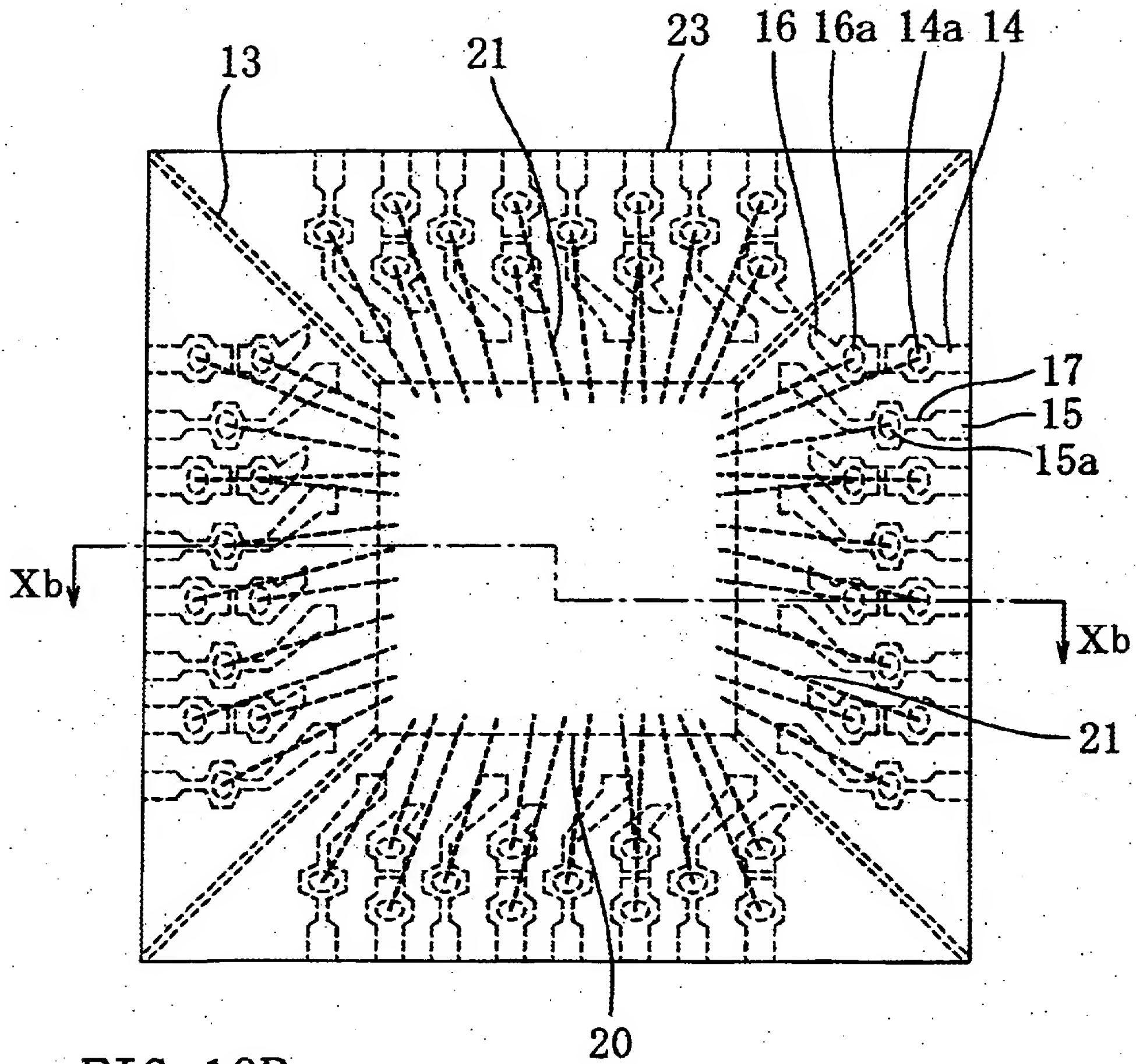


FIG. 10B

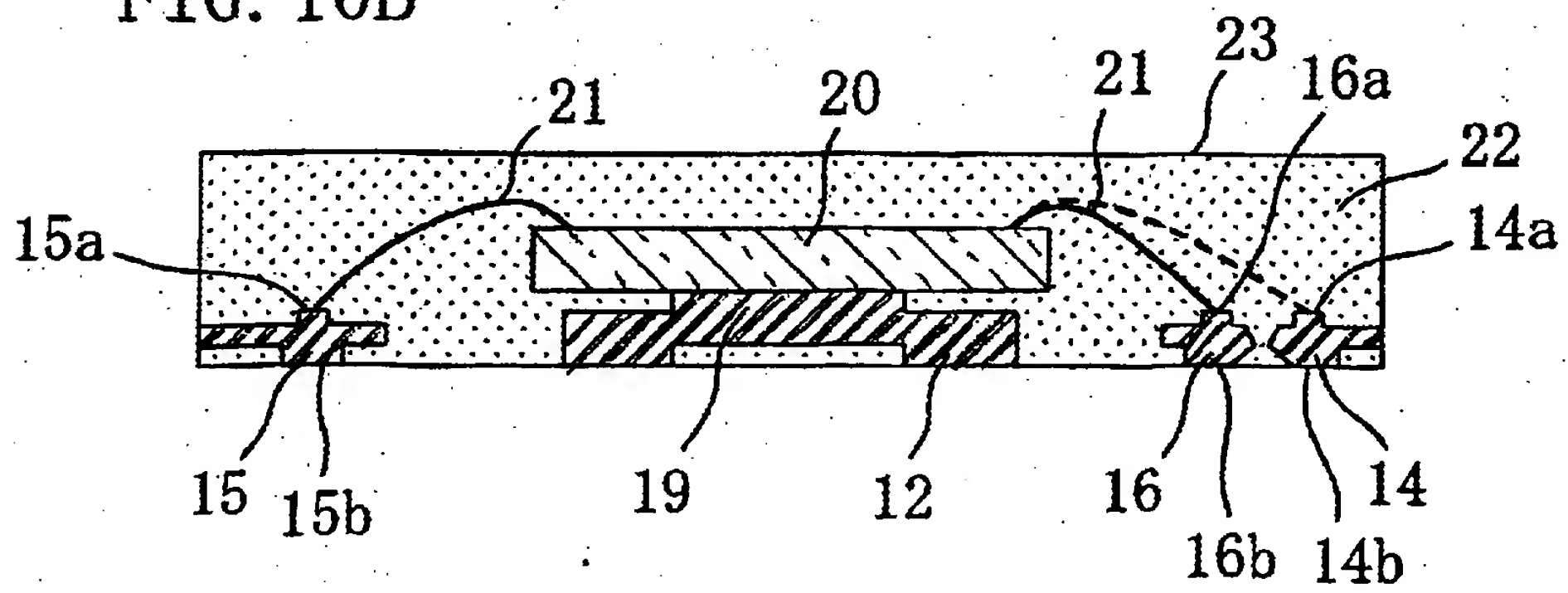




FIG. 11
PRIOR ART

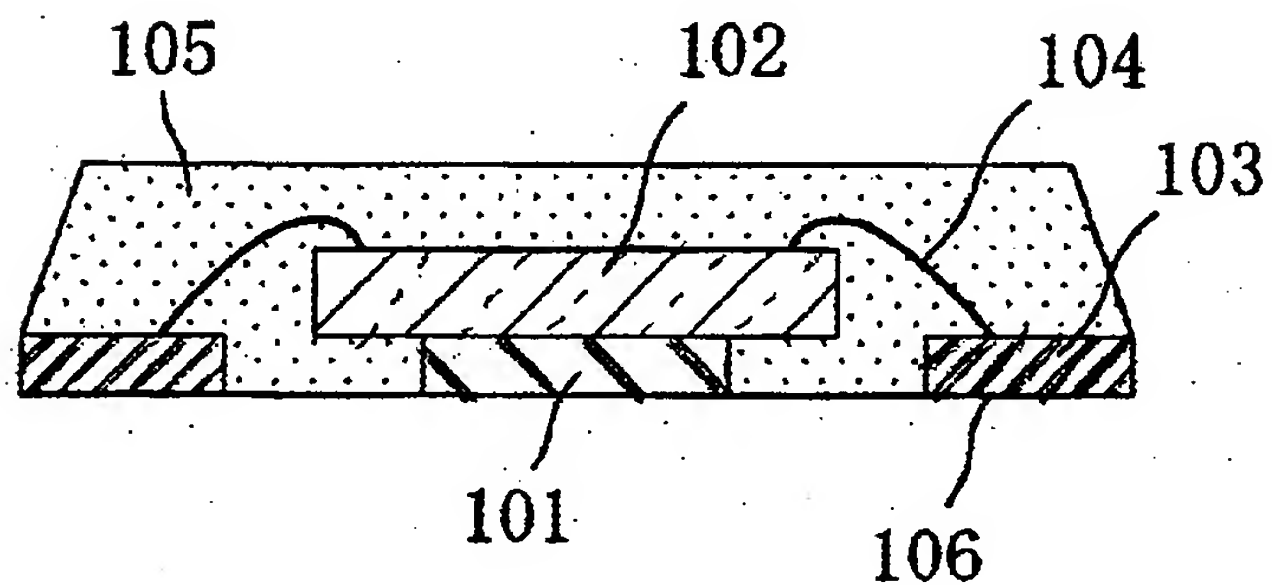


FIG. 12
PRIOR ART

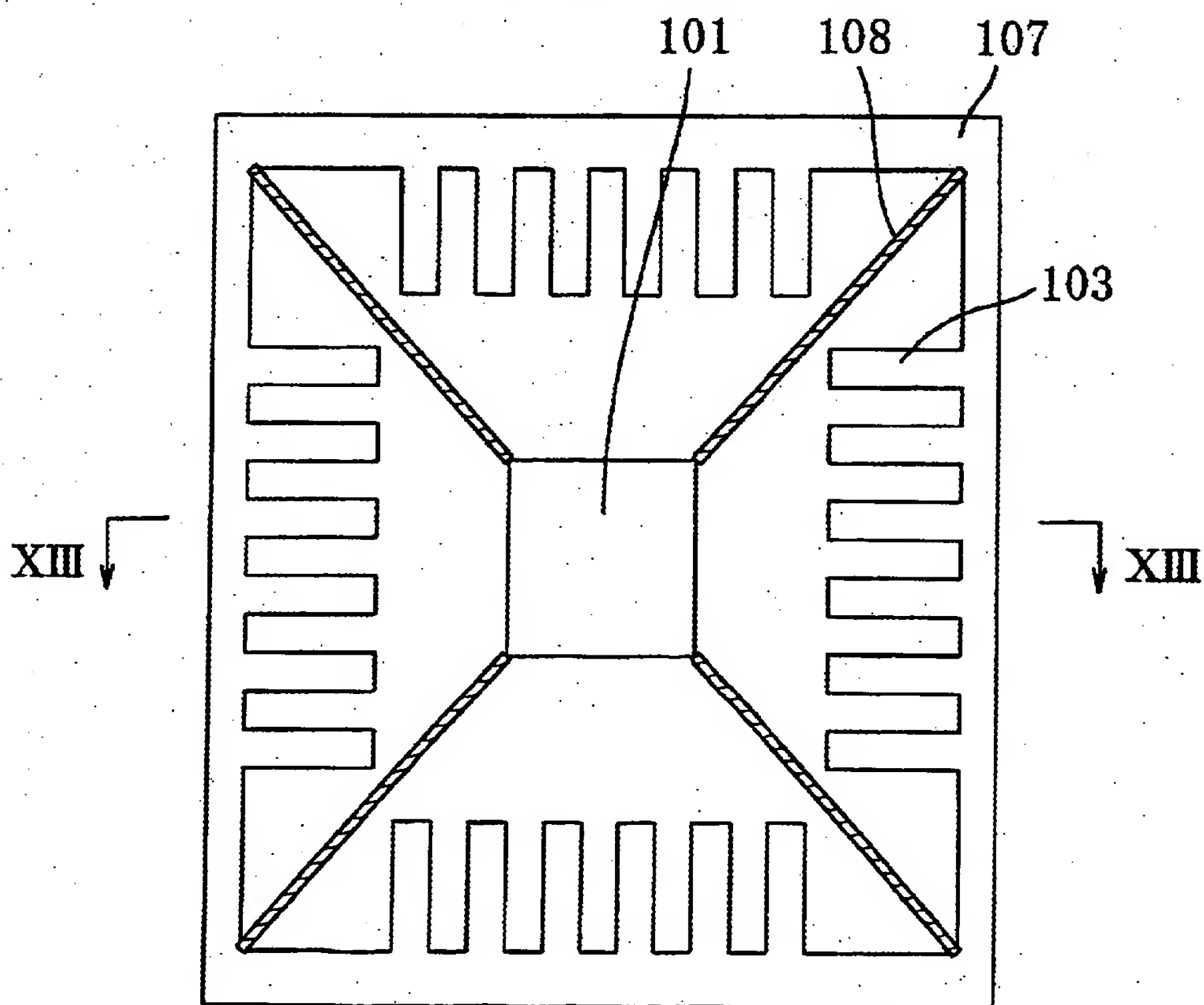




FIG. 13A

PRIOR ART

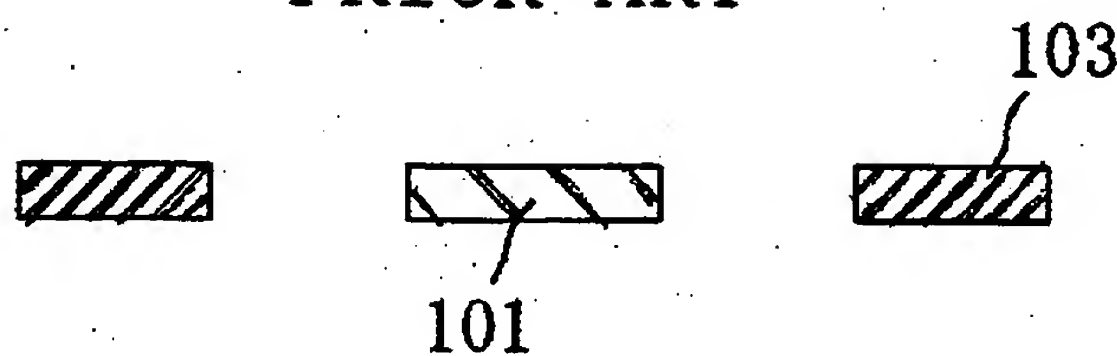


FIG. 13B

PRIOR ART

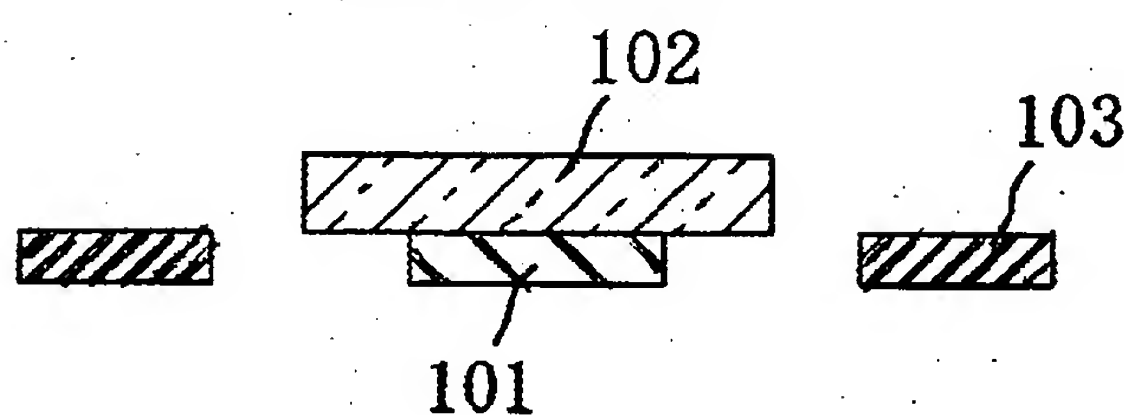


FIG. 13C

PRIOR ART

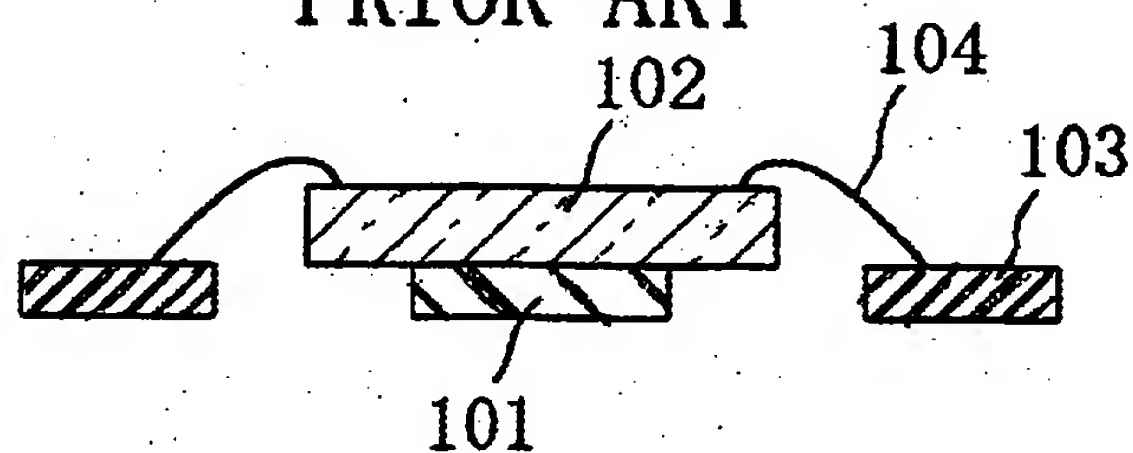


FIG. 13D

PRIOR ART

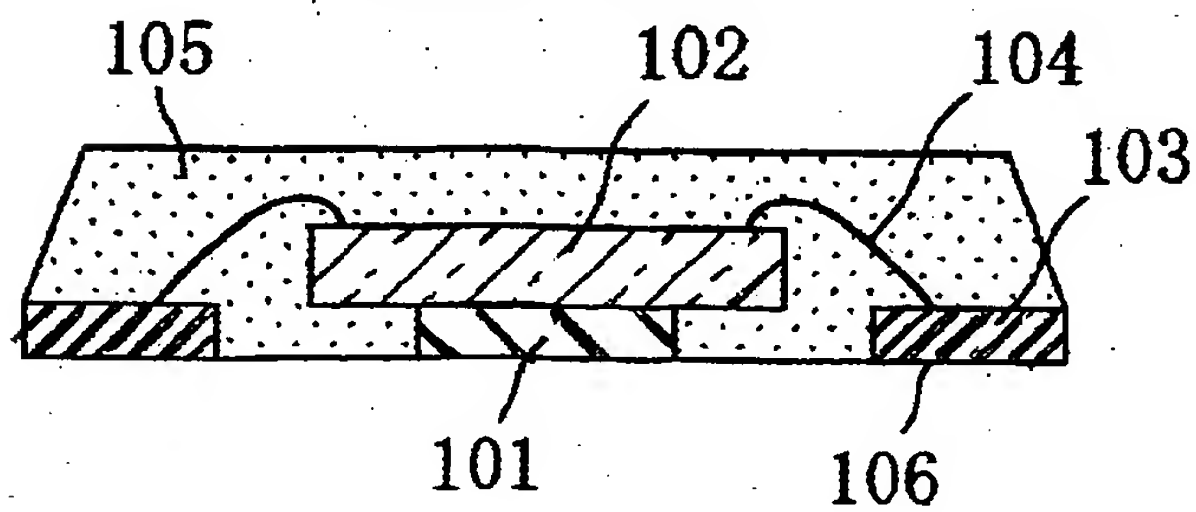




FIG. 14A
PRIOR ART

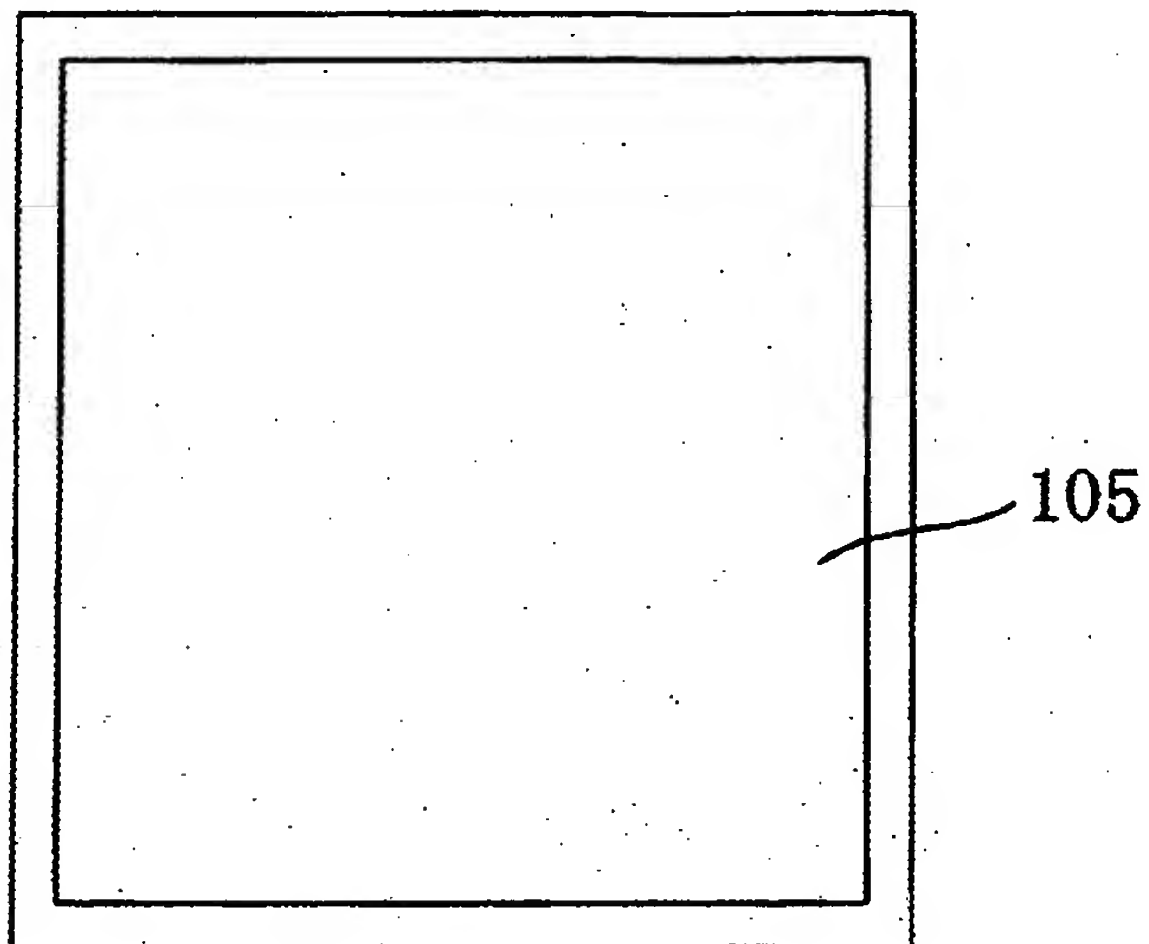


FIG. 14B
PRIOR ART

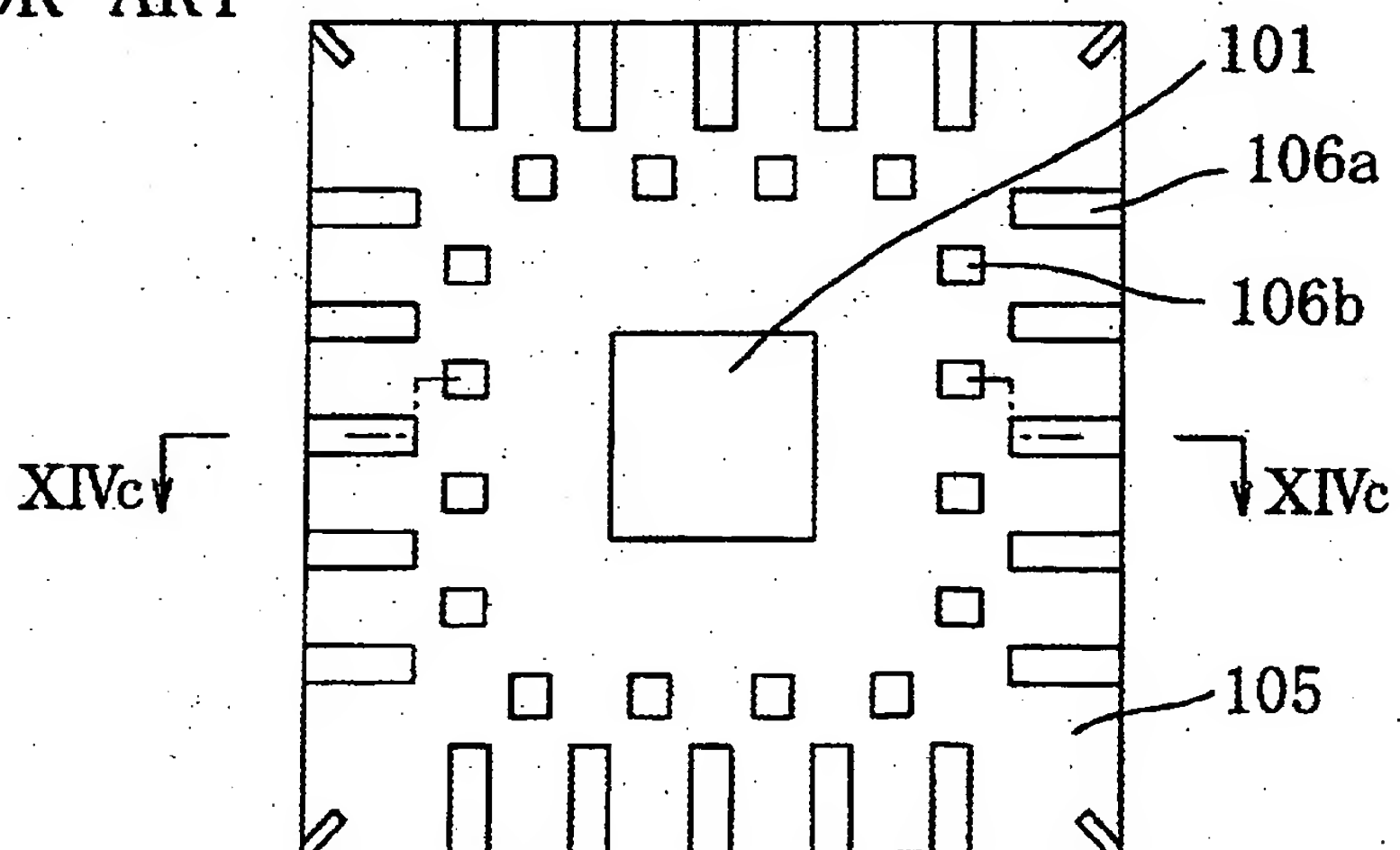


FIG. 14C
PRIOR ART

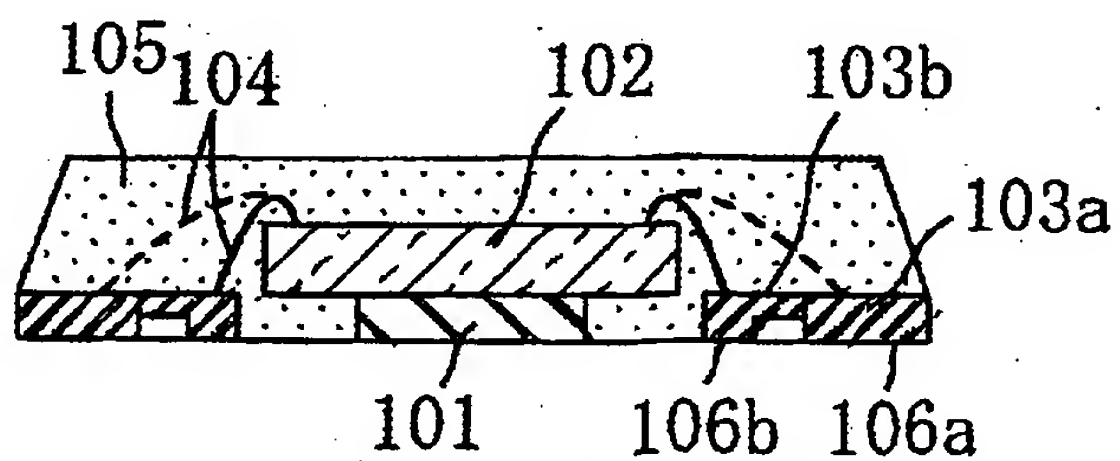




FIG. 16A

PRIOR ART

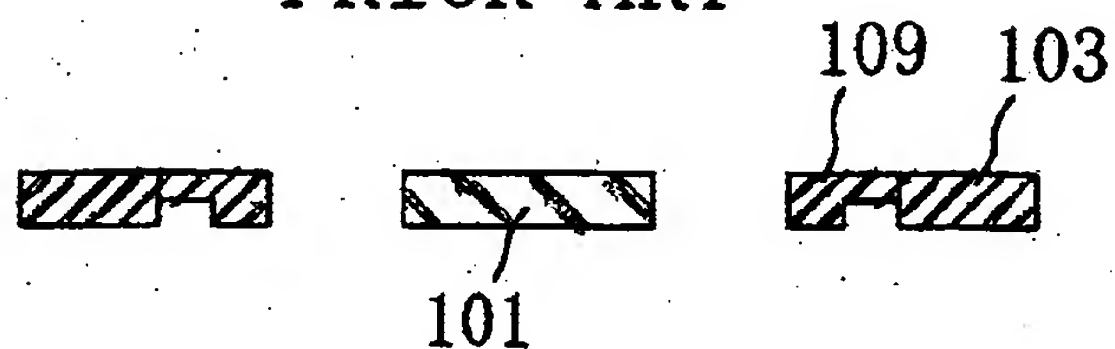


FIG. 16B

PRIOR ART

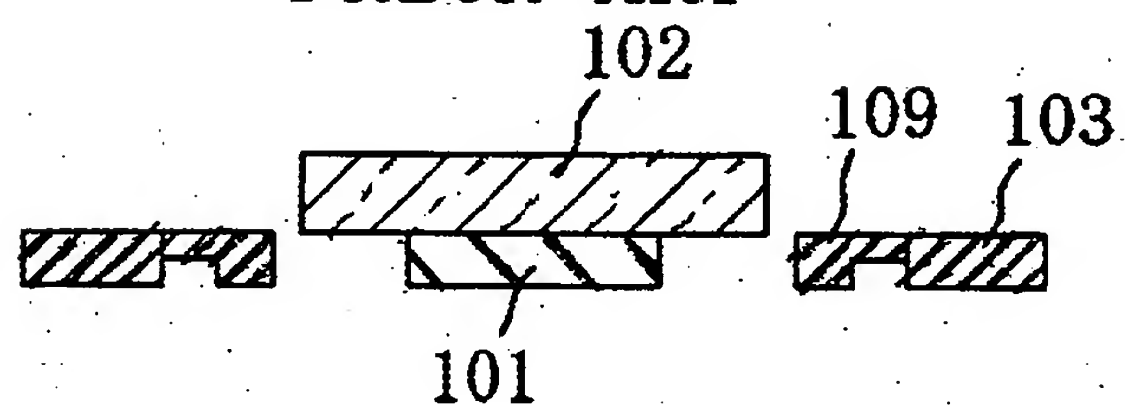


FIG. 16C

PRIOR ART

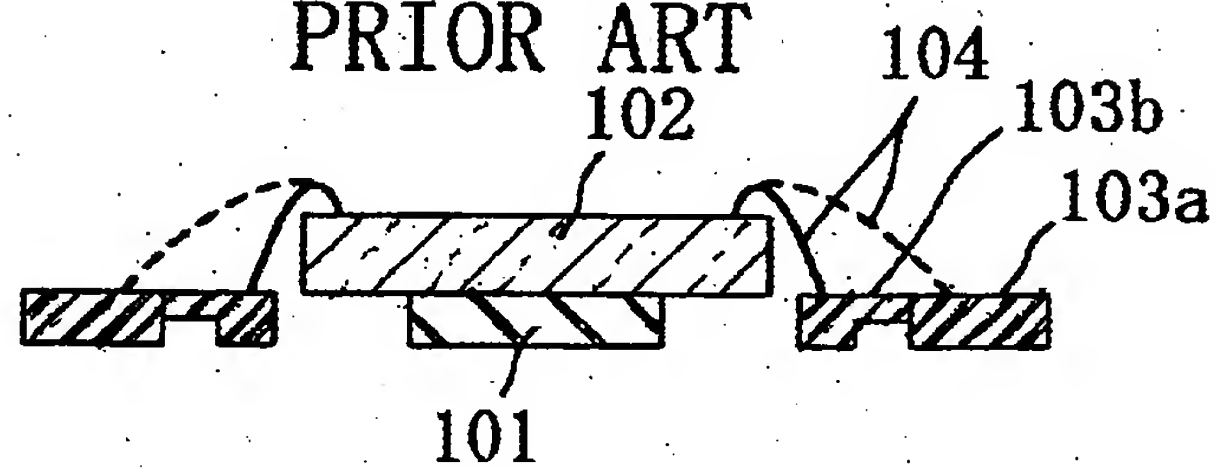


FIG. 16D

PRIOR ART

